Student Name: Aman Roll Number: 21332

Indian Institute of Information Technology, Lucknow
End Semester Examination
(Computer Organization and Architecture - COA2004C)

Maximum Marks: 70 **Maximum Time: 3 Hours**
Date: 8th May, 2024 **Instructor: Dr. Niharika Anand**

Answer All the Questions. All parts of the questions must be answered consecutively. Show your calculations corresponding to the answers on the answer sheet only. Rough calculations will not be accepted.

1. COMMON DATA FOR (a) and (b)

A pipelined processor uses a 4-stage instructions pipeline with the following stages. Instruction fetch (IF),Instruction decode (ID),execute(EX) and write back (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement

X = (S-R*(P+Q)) / T is given below:

The values of variables P,Q,R,S and T are available in the register R_0, R_1, R_2 and R_4 respectively; before the execution of the instruction sequence.

ADD	R_5,R_0,R_1;	$R_5 \leftarrow R_0 + R_1$
MUL	R_6,R_2,R_5;	$R_6 \leftarrow R_2 * R_5$
SUB	R_5,R_3,R_6;	$R_5 \leftarrow R_3 - R_6$
DIV	R_6,R_5,R_4 ;	$R_6 \leftarrow R_5 / R_4$
STORE	R_6,X ;	$X \leftarrow R_6$

a.) What will be the number of read-after-write (RAW),write-after-read (WAR) and write-after-write (WAW) dependencies in the sequence of instructions. (5)

b.) The IF,ID and WB stages take 1-clock cycle each. The EX stage takes 1 -clock cycle each for the ADD,SUB and STORE operations and 3-clock cycles each for MUL and DIV operations. Operand forwarding from the EX stage to the ID stage is used. Elaborate the number of clock cycles required to complete the sequence of instructions. (5)

2. COMMON DATA FOR (a) and (b)

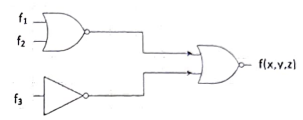
Consider the 5-stage pipeline which allows overlapping of all instructions except branch instruction. The target of branch instruction is not available until the branch instruction is completed. Let each stage delay is 20 ns and there are 30% branch instruction.

a.) What is the average instruction execution time (ignore the fact that some of them are conditional)? (in ns) (3)

b.) What is the performance gain of the pipeline over nonpipelining? (2)

c.) Among the branch instructions, 30% are conditional and 70% of them does not satisfy the condition (branch not taken). If there is no stall due to them. What is average instruction execution time (in ns)? (5)

3.



If $f_1(x, y, z) = \sum m(0, 1, 3, 5)$,
$f_2(x, y, z) = \sum m(4, 5)$ and
$f(x, y, z) = \sum m(1, 4, 5)$

Then find $f_3(x,y,z)$? (5)

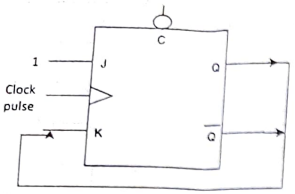
4. Design a PLA and PAL to implement the following functions:
a) X(A,B,C)=A'B+A'BC+ABC'
b) Y(A,B,C)=A'B'C+ABC+AB'C' (3.5+3.5)

5. How many minimum number of 2 input NAND gates required to realise full substractor? Explain the reason in detail. (5)

6. A 4-bit carry lookahead adder, which adds two End 4-bit numbers, is designed using AND, OR, NOT. NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate in one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic. Show the gate diagram also for the solution. (5)

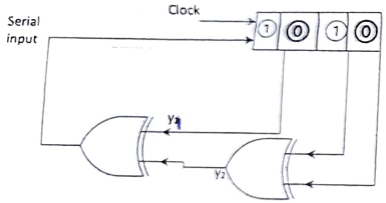
7. Consider the multiplexer with X and Y as data inputs and Z as control input. Z=0 selects input X and Z=1 selects input Y. Show the connections required to balance the 2-variable Boolean function f=T+R without using any additional hardware? (3)

8. In figure, assume that initially Q=1 with clock pulses being given,What will be the subsequent states of Q ?



(3)

9. The shift register shown in the given figure is initially loaded with the bit pattern 1010. Subsequently, the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (msb). After how many clock pulses will the content of the shift register become 1010 again?



(2)

10. Draw the Block diagram of the Stack Organisation and explain its operation in detail. **(A+B/C*(D+E)-F)** Scan the given characters into Postfix using Stack. **(5)**

11. X= [A- B + C(D* E-F)]/(G+H*K) ; Write the instruction program to evaluate the arithmetic expression using **Three address, Two address, One address and Zero address.** **(5)**

12. **a.)** Differentiate between **RISC** and **CISC** architecture using clock pulse cycle with the condition of delay load. **(2)**

b.) Draw a memory connection chip diagram of RAM and ROM to the CPU defining each operation with a balanced **Hexadecimal addresses.** **(3)**

13. a.) Draw a flowchart explaining the Booth Multiplication algorithm with a suitable example. **(3)**

b.) The frequency of different types of instruction executed by a machine is tabulated below

Operand Accessing	**Mode Frequency in %**
Register	30
Immediate	20
Direct	22
Memory indirect	17
Index	11

Assuming two cycles are consumed for an operand to be read from the memory, one cycle for index arithmetic computation and zero cycles for the operands available in registers or in the instruction itself,find the average operand fetch rate of the machine ? **(2)**